direction, in which the embedded second conductive type region extends, the contact second conductive type region easily contacts the embedded second conductive type region, compared with a case where the contact second conductive type region extends along with the first direction as the extending direction of the embedded second conductive type region. Thus, the shift of alignment of the contact second conductive type region and the embedded second conductive type region is reduced.

[0147] Further, the embedded second conductive type region may be divided into a plurality of embedded second conductive type region portions along with the first direction. The embedded second conductive type region portions are separated from each other by a predetermined interval, and each embedded second conductive type region portion is disposed under the contact second conductive type region. In this case, since the embedded second conductive type region portions contacting the trenches is not formed in the channel layer, the current path disposed between the channel layer and the first conductive type region is restricted from being blocked by the embedded second conductive type region portions. Thus, the increase of the on-state resistance is improved.

[0148] Alternatively, the semiconductor device may further include: a cell portion; and an outer periphery portion. The current flows between the surface electrode and the backside electrode in the cell portion. The outer periphery portion surrounds the cell portion. The trenches in the cell portion extend in the first direction. The embedded second conductive type region in the cell portion and the outer periphery portion extends in the first direction. The embedded second conductive type region has an end in the outer periphery portion, which is disposed on an outer side of an end of the trench in the first direction. In this case, the electric field concentration is restricted from occurring at the end of the trench in the extending direction, compared with a case where the embedded second conductive type region has the end, which is disposed on the inside of the end of the trench.

[0149] Further, the embedded second conductive type region may be divided into a plurality of embedded second conductive type region portions along with the first direction. The embedded second conductive type region portions are separated from each other by a predetermined interval. In this case, the embedded second conductive type region portions are not partially formed, and therefore, the current path, in which the embedded second conductive type region portions are not formed, is not narrowed by the embedded second conductive type region portions. Thus, the breakdown voltage is held, and the on-state resistance is reduced.

[0150] According to a second aspect of the present disclosure, a method for manufacturing a semiconductor device includes: forming a first conductive type region film on a substrate having a first conductive type; forming a plurality of first trenches on the first conductive type region film to reach the substrate so that the first conductive type region film is divided into a plurality of first conductive type regions, which are separated from each other with the first trenches; filling each first trench with a second conductive type region film; polishing a surface of the second conductive type region film so that the second conductive type region film is divided into a plurality of second conductive type regions, and the first conductive type regions and the second conductive type regions provide a super junction structure, wherein the first conductive type regions and the second conductive type regions extend in a first direction, and wherein the first conductive type regions and the second conductive type regions are alternatively arranged in a second direction; implanting a second conductive type impurity into the second conductive type regions; forming a channel layer having a second conductive type on the super junction structure; forming a plurality of second trenches to penetrate the channel layer and to reach a corresponding first conductive type region, wherein the second trenches have a stripe pattern; forming a gate insulation film on an inner wall of each second trench, and forming a gate electrode on the gate insulation film in each second trench, so that the second trenches, the gate insulation film and the gate electrode provide a trench gate structure; implanting a first conductive type impurity into a surface portion of the channel layer; implanting a second conductive type impurity into another surface portion of the channel layer; and heating the substrate so that the second conductive type impurity in the channel layer is diffused, and a contact second conductive type region is formed in the another surface portion of the channel layer, which is opposite to a corresponding second conductive type region. The contact second conductive type region has an impurity concentration higher than the channel layer. In the heating of the substrate, the first conductive type impurity in the channel layer is diffused, and a first conductive type layer is formed in the surface portion of the channel layer. The first conductive type layer has the first conductive type, and contacts a sidewall of a corresponding trench. In the heating of the substrate, the second conductive type impurity in the second conductive type regions is diffused, and an embedded second conductive type region is formed in a corresponding second conductive type region. The embedded second conductive type region has an end, which protrudes into the channel layer and contacts the contact second conductive type region. The embedded second conductive type region has the other end, which is deeper than a bottom of a corresponding trench. The embedded second conductive type region has an impurity concentration higher than the channel layer, and has a maximum impurity concentration at a position in the corresponding second conductive type region.

[0151] In the above method, the second conductive type impurity is implanted in the second conductive region, so that the embedded second conductive type region is formed after the heat treatment. Accordingly, the thermal treatment temperature is low, and the thermal treatment time is short, compared with a conventional case where the second conductive type impurity is implanted in the channel layer, and the embedded second conductive type region is formed to reach the second conductive type region after the heat treatment. Thus, the charge balance between the first and second conductive type regions is not changed.

[0152] According to a third aspect of the present disclosure, a method for manufacturing a semiconductor device includes: forming a first conductive type region film on a substrate having a first conductive type; forming a plurality of first trenches on the first conductive type region film to reach the substrate so that the first conductive type region film is divided into a plurality of first conductive type regions, which are separated from each other with the first trenches; filling each first trench with a second conductive type region film, and forming the second conductive type region film on the first conductive type regions; implanting a second conductive type impurity into the second conductive type region film in each trench with using the second conductive type region film on the first conductive type regions as a mask; polishing a surface of the second conductive type region film so that the second conductive type region film is divided into a plurality of second conductive type regions, and the first conductive type regions and the second conductive type regions provide a super junction structure, wherein the first conductive type